

1 (C) AMENDMENTS TO THE CLAIMS

2 1. (Cancelled.)

3 2. (Currently Amended) The structure as set forth in claim [[1]] 4 wherein said at
4 least one same metallization layer further comprises a top metal layer of at least one of
5 said die.

6 3. (Cancelled.)

7 4. ~~[[The structure as set forth in claim 3]]~~

8 An integrated circuit structure including chip-scale packaging, the structure
9 comprising:

10 _____ in a wafer-scale integrated circuit device wherein a first die has at least one first
11 input-output bump, first associated redistribution beam and first associated die pad, and
12 a second die has at least one second input-output bump, second associated
13 redistribution beam and second associated die pad,

14 _____ an electrical interconnect between the first die and the second die wherein the
15 electrical interconnect uses at least one same metallization layer for forming each said
16 redistribution beam, and

17 _____ for a plurality of more than two dice and a plurality of electrical interconnects
18 between said plurality of more than two dice, using the at least one same metallization
19 layer for each die electrical interconnect.

20 5. (Currently Amended) The structure as set forth in claim [[4]] 4 wherein said
21 structure is formed on a wafer having scribe line region between said first die and said
22 second die, a polyimide-like bridge across said region and superjacent an active
23 component surface of said first die and said second die and subjacent said at least one
24 same metallization layer.

1 6. (Canceled.)

2 7. (Currently Amended) [~~The integrated circuit chip set as set forth in claim 6~~]

3 An integrated circuit chip set comprising:

4 in a wafer-scale integrated circuit device, a plurality of discrete integrated circuit
5 devices, each of said devices including discrete circuit elements and associated input-
6 output pads, wherein each of said devices includes chip-scale bump input-output
7 terminals connected by conductive material layer beams to the electrical pads, and
8 electrical traces connecting said discrete integrated circuit devices wherein said
9 electrical traces are concomitant with the conductive material layer forming the beams.

10 8. (Currently Amended) The integrated circuit chip set as set forth in claim [[6]] 7
11 further comprising:

12 a dielectric material layer subjacent said electrical traces.

13 9. (Currently Amended) The integrated circuit chip set as set forth in claim [[6]] 7
14 wherein said plurality of discrete integrated circuit devices are connected in parallel via
15 said electrical traces.

16 10. (Currently Amended) The integrated circuit chip set as set forth in claim [[6]] 7
17 wherein said plurality of discrete integrated circuit devices are connected in via said
18 electrical traces such that said traces are formed concurrently with a top metal layer of
19 said discrete integrated circuit devices.

20 11. (Canceled)

21 12. (Canceled)

22 13. (Canceled)

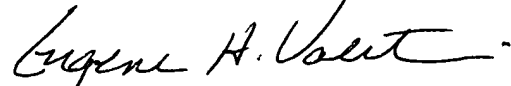
1 (D) REMARKS, including DRAWING AMENDMENTS, if any

2 Applicant is in disagreement with the rejections enumerated in the Office Action. However,
3 Claims 4 and 7 were deemed allowable by the Office. The foregoing amendments render
4 rejections of the remaining claims moot. Based upon the foregoing, it is submitted that the
5 application now presents claims which are directed to novel, unobvious and distinct features of
6 the present invention which are an advancement to the state of the art. Reconsideration and
7 early allowance of all claims is respectfully requested. The right is expressly reserved to
8 reassert any and all arguments, including the raising of new arguments, should a Notice of
9 Allowance not be forthcoming.

10 Questions or suggestions that will advance the case to allowance may be directed to the
11 undersigned by teleconference at the Examiner's convenience.

12 Date: Nov. 2, 2004
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Respectfully submitted,
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